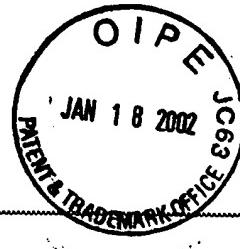


Dialog



Semiconductor device mfg. process - involves cold welding of ramps to mould surface before pouring resin, to prevent resin film formation on ramp surface
Patent Assignee: MITSUBISHI ELECTRIC CORP

Patent Family

Patent Number	Kind	Date	Application Number	Kind	Date	Week	Type
JP 6151487	A	19940531	JP 92302501	A	19921112	199426	B

Priority Applications (Number Kind Date): JP 92302501 A (19921112)

Patent Details

Patent	Kind	Language	Page	Main IPC	Filing Notes
JP 6151487	A		4	H01L-021/56	

Abstract:

JP 6151487 A

The method deals with semiconductor elements with ramps which are to be sealed with resin. Usually, the semiconductor element (1) with ramps (3) formed on electrodes (2) is enclosed in a mould and is filled with resin which hardens. If the height of the upper part of the mould is not properly maintained with respect to the height of the ramp, a clearance is formed between the upper surface of the ramp and the upper mould surface. This causes a layer of resin to be formed on the ramp surface. This is avoided by first cold-welding the ramps to the upper mould surface and by maintaining the height of the upper mould less than the height of the ramps. Thus, any clearance between mould surface and ramp is avoided, thereby preventing resin coating on ramp surfaces.

ADVANTAGE - Semiconductor devices with ramps are sealed with resin effectively.

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